REMARKS

Claims 1, 3, 7, 9, 13, 15, 19, and 21have been amended. No claims have been canceled. No new claims have been added. Claims 1-24 are pending.

The specification has been objected to due to the use of attorney docket number to identify related applications. The specification has been revised to refer to applications by serial number. Accordingly, the objection to the specification should be withdrawn.

Claims 1-24 stand rejected under 35 U.S.C. 102(b) as being anticipated by Draves (U.S. Patent No. 6,349,355). This rejection is respectfully traversed.

Claim 1 recites, *inter alia,* "accessing said function via said identifier in said privileged and non-privileged modes."

Claim 7 recites, *inter alia,* "logic for accessing said function via said identifier in said privileged and non-privileged modes."

Claim 13 recites, *inter alia,* "means for accessing said function via said identifier in said privileged and non-privileged modes."

Claim 19 recites, *inter alia,* "instructions for accessing said function via said identifier in said privileged and non-privileged modes."

Draves is directed to a computer system in which the user virtual address space is mapped to an offset of the kernel address space. When a kernel function is called, data passed to the kernel function by reference (e.g., via a pointer) is biased to accommodate the offset before dereferencing, thereby permitting the sharing of position dependent code while simultaneously permitting the kernel access to the user memory space.

Draves discloses that on some computer systems with non-segmented memory addressing architecture, such as the MIPS family of processors, the translation lookaside buffer (TLB), a cache of the mapping between real and virtual addresses stored in the page tables, is software

manageable and are indexed by identifiers known as an address space identifiers (ASIDs). That is, each ASID is a pointer to a TLB entry.

Draves discloses associated each process with a pair of ASIDs and TLB entries. A first ASID pointing to a first TLB entry would be used for user mode operations, while a second ASID pointing to a second TLB entry would be used for kernel mode operations. Dravis therefore discloses using two TLB entries for a function to accommodate the addressing differences between the user and kernel modes. Dravis fails to disclose or suggest the use of an identifier for accessing the function in both privileged and non-privileged modes as recited in the above quoted portions of independent claims 1, 7 13, and 19.

Claims 3, 9, 15, and 21 have been rewritten as independent claims. Claims 3, 9, 15, and 21 each recite "wherein the data structure is a table that maps identifiers to functions." As noted above, the data structure associated with each identifier in Draves is the TLB. Since a TLBs map between real and virtual addresses, and not between identifiers and functions, Dravis fails to disclose or suggest a "table that maps identifiers to functions," as recited in each of independent claims 3, 9, 15, and 21.

Accordingly, claims 1, 3, 7, 9, 13, 15, 19, and 21 are believed to be allowable over the prior art of record. The depending claims (i.e., claims 2, 4-6, 8, 10-12, 14, 16-18, 20, and 22-24) believed to be allowable for at least the same reasons as the independent claims.

CONCLUSION

In light of the amendments contained herein, Applicants submit that the application is in condition for allowance, for which early action is requested.

Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

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